IN THE CLAIMS

Please enter the following indicated amendments.

1. (Withdrawn)
2. (Withdrawn)
3. (Withdrawn)
4. (Withdrawn)
5. (Withdrawn)
6. (Withdrawn)
7. (Withdrawn)
8. (Currently Amended) An SEU-resistant circuit comprising

a logic gate having an input and an output;

a feedback path from the output of the logic gate to the input of the logic gate, the feedback path comprising two or more [delay] logic elements, said logic gate and said two or more logic elements each comprising an input to output pulse response operable for delaying a propagation time of a pulse propagating therethrough and for selectively reducing a pulse width thereof; and

the logic gate and the two or more [delay] logic elements being [configured to absorb a standard] operable for reducing in size an instance of a potentially SEU producing glitch introduced at the input [to] of the logic gate before [it] the potentially SEU producing glitch propagates through the feedback path to the input of the logic gate, the input to output pulse response of the logic gate and the two or more logic elements being substantially similar in that the resulting amount of pulse propagation delay and amount of reduction of the pulse width of

the potentially SEU producing glitch [being] is spread substantially evenly among the logic gate and the two or more [delay] logic elements.

9. (Cancelled).

10. (Currently Amended) The SEU-resistant circuit of claim 8 wherein [the delay elements comprise balanced gates] the input to output pulse response of the logic elements is balanced such that a rise time and fall time of the input to output pulse response is approximately the same for each of the logic elements.

11. (Currently Amended) The SEU-resistant circuit of claim 8 [wherein the feedback path further comprises a driver gate] further comprising a plurality of logic gates, an input to output pulse response of the plurality of logic gates and the two or more logic elements being configured to produce a pulse propagation delay approximately no longer than a maximum pulse propagation delay of the slowest of the plurality of logic gates when the slowest logic gate is fully loaded with maximum fan out.

12. Currently Amended) The SEU-resistant circuit of claim [8] 11 wherein [the delay elements comprise inverters] the input to output pulse response of the plurality of logic gates and each of the two or more logic elements is operable to prevent a glitch with a time length less than approximately one-half of the maximum pulse propagation delay from passing through the plurality of logic gates or through each of the two or more logic elements without being reduced in size such that said glitch is unable to trigger a subsequent logic element.

13. (Currently Amended) The SEU-resistant circuit of claim [8] 11 wherein [the number of delay elements is even] the input to output pulse response of the plurality of logic gates and the two or more logic elements does not substantially reduce the time length of a pulse with a time length greater than two times the maximum pulse propagation delay.

14. (Withdrawn)

15. (Withdrawn)

16. (Withdrawn)

22. (Withdrawn)

23. (Withdrawn)

24. (Withdrawn)

25. (Withdrawn)

26. (Withdrawn)

27. (Withdrawn)

28. (Withdrawn)

29. (Withdrawn)

30. (Currently Amended) A method for reducing the vulnerability of an [latch] electronic circuit to single event upsets, comprising: [the latch comprising a gate having an input and an output and a feedback path from the output to the input of the gate, the method comprising]

providing one or more logic gates for said circuit with a feedback path from an output of a respective of the one or more logic gates to an input thereof;

inserting [a delay] one or more logic elements into the feedback path; and

providing [a delay in the] that the one or more logic circuits and the one or more logic gates each have an input to output pulse response such that an initial input glitch with a pulse width less than a pulse width L1 effectively does not pass through a respective of

the one or more logic circuits or a respective of the one or more logic gates because a resulting diminished output glitch is not capable of triggering a change of state of a subsequent logic element; and

providing that if the initial input glitch has a pulse width greater than pulse width L1 but less than a pulse width L2 then the resulting diminished output glitch effectively passes through the respective of the one or more logic circuits or the respective of the one or more logic gates because the resulting output glitch is then capable of triggering a change of state of the subsequent logic device but that the resulting diminished output glitch then has a reduced pulse width as compared to the initial input glitch; and

providing that the pulse width L1 and the pulse width L2 are approximately equal for the respective of the one or more logic circuits and for the respective of the one or more logic gates.

31. (Currently Amended) The method of claim 30 wherein the one or more logic gates comprise[s] a first FET [having] comprising a first channel and a second FET [having] comprising a second channel, [the channel of the first FET and the channel of the second FET coupled at a node having a parasitic capacitance], wherein said providing step comprises:

adjusting the characteristics of the first channel of the first FET[, the characteristics of the channel of the second FET and the parasitic capacitance of the node].

32. (Currently Amended) The method of claim 31 wherein said step of adjusting comprises [increasing] changing at least one of a width or [the] a length of the first channel of the first FET.

33. (Currently Amended) The method of claim 32 wherein [increasing] said step of changing comprises making the first channel [non-linear] wider.

34. (Currently Amended) The method of claim [33] 31 wherein said step of adjusting [making] comprises inserting a [jog] non-linearity into the first channel.

35. (Currently Amended) The method of claim 34 wherein the [jog] non-linearity is a right angle.

36. (Currently Amended) The method of claim 31 [further comprising:] wherein an input signal pulse having a signal pulse width greater than a pulse width L3 effectively passes through the respective one or more logic gates or passes through the respective one or more logic circuits without a substantial change in a resulting output signal pulse width.

[coupling the output of the gate to a threshold device having an input, an output and a threshold, the output having a first value when the input is less than the threshold and a second value when the input is greater than the threshold.]

37. (Currently Amended) The method of claim 31 further comprising:

providing that said one or more logic gates and the one or more logic circuits comprises a latch circuit.

[adjusting the time constant and the threshold so that

a glitch of length L1 at the input to the gate would not effect the output of the threshold device;

a glitch of length L2, L1 <L2 <L3, would cause a pulse of length L4 <L2 to appear at the output of the threshold device after a delay determined by the time constant and the threshold; and

a glitch of length L5 > L3 would cause a pulse of length approximately L5 to appear at the output of the threshold device after a delay determined by the time constant and the threshold.]